ABSTRACT OF THE DISCLOSURE

There is provided an EEPROM semiconductor device including (a) a plurality of field insulating films each extending perpendicularly to word lines, (b) a plurality of memory cells arranged in a matrix, each memory cell having a floating gate, a control gate formed on the floating gate and doubling as a word line, and source and drain regions located at either sides of the control gate, (c) a common source line extending in parallel with the word lines and connecting source regions of the memory cells with each other, and (d) a first bit line extending perpendicularly to the word lines and connecting drain regions of the memory cells with each other. The above-mentioned EEPROM semiconductor device makes it possible to form CMOS logic circuit together with a non-volatile memory on a common semiconductor substrate without increasing fabrication steps, and also makes it possible for the non-volatile memory to write data thereinto and read data therefrom at a higher rate without an increase in a cell size.